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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,803	02/08/2001	Moinul I. Syed	A0312/7378 (RMA)	5583
7590	02/02/2004		EXAMINER	LI, ZHUO H
William R. McClellan c/o Wolf, Greenfield & Sacks, P.C. Federal Reserve Plaza 600 Atlantic Avenue Boston, MA 02210-2211			ART UNIT	PAPER NUMBER
			2186	
			DATE MAILED: 02/02/2004	7

Please find below and/or attached an Office communication concerning this application or proceeding.

P24

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/779,803	SYED ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 31 October 2003.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-45 is/are pending in the application.
- 4a)  Of the above claim(s) 8-29 and 43-45 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-7 and 30-42 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) The translation of the foreign language provisional application has been received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____ .

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election with traverse of Group I in Paper No. 6 is acknowledged. The traversal is on the ground(s) that a search and examination of all claims would place no undue burden on the Examiner. This is not found persuasive because Group I, Group II and Group II are related as subcombinations disclosed as usable together in a single combination so that the search required for Group I is not required for Group II and Group III. In addition, Group I, Group II and Group III have acquired a separate status in the art as shown by their different classification, thereby restriction for examination purpose as indicated as proper.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 8-29 and 43-44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 6.

3. This application contains claims 8-29 and 43-44 are drawn to an invention nonelected with traverse in Paper No. 6. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6-7, 30-31, 34-35 and 41-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Cypher (US PAT. 6,289,420).

Regarding claim 1, Cypher discloses a cache memory system comprising a plurality of memory locations (160A to 160N, figure 1) for storing data (107, figure 2) and address associated with the data (105, figure 2), each of the plurality of memory locations having only a single word line associated therewith (figure 3), at least one controller (140, figure 1) that enables first and second devices to access different ones of the plurality of memory location concurrently (col. 3 line 66 through col. 6 line 65).

Regarding claim 2, Cypher discloses the memory locations being configured and arranged to be included in at least first and second ways, wherein the at least one controller is configured and arranged to enable the first and second device to concurrently access memory locations included in the first and second ways, respectively (col. 5 lines 9-36 and col. 5 line 66 through col. 6 line 10).

Regarding claim 3, Cypher teaches the at least one controller being configured and arranged to give the first and second devices exclusive access to the first and second ways respectively (col. 6 lines 24-65).

Regarding claim 6, Cypher discloses a cache memory system comprising a plurality of memory locations (106A to 106N, figure 1) to store data (107, figure 2) and addresses associated with the data (105, figure 2), a plurality of cache outputs (TAG A to TAG N, figure 4) for providing data retrieved from the memory locations, and first and second multiplexers having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs so as to enable the first and second multiplexers to select data from different ones of the plurality of memory locations to be provided concurrently on respective ones of the plurality of cache outputs (col. 3 line 66 through col. 6 line 65).

Regarding claim 7, Cypher teaches some of the memory locations being configured and arranged to form a data array having at least two ways, with each of the at least two ways having a respective data array output for providing data retrieved therefrom, and the multiplexer inputs of the first and second multiplexers being coupled to the data array outputs so as to enable the first and second multiplexers to concurrently select data from different ones of the at least two ways of the data array provided concurrently on respective ones of the plurality of cache outputs (col. 3 line 66 through col. 6 line 65).

Regarding claim 30, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 34, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 35, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 41, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 42, the limitations of the claim are rejected as the same reasons set forth in claim 2.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4-5 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cypher (US PAT. 6,289,420) in view of Malamy et al. (US PAT. 5,675,765 hereinafter Malamy).

Regarding claims 4-5, Cypher teaches the first device including a processor configured and arranged to access memory locations (col. 5 lines 44-50). Cypher differs from the claimed invention in not specifically teaching the second device including a data transfer engine comprising a DMA controller being configured and arranged to transfer data between the memory locations and a lower level memory. However, Malamyy teaches a cache memory system with independently accessible subdivided cache tag array comprising a DMA controller to transfer data between the memory location and a lower level memory (col. 4 lines 8-19) in order to perform two independent cache operations concurrently on a multiprocessor system, thereby reducing operation time. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Cypher in having the second device including a data transfer engine comprising a DMA controller being configured and arranged to transfer data between the memory locations and a lower level memory, as per teaching of Malamy, in order to perform two independent cache operations concurrently on a multiprocessor system, thereby reducing operation time.

Regarding claims 32-33, the limitations of the claims are rejected as the same reasons set forth in claims 4-5.

8. Claims 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cypher (US PAT. 6,289,420) in view of Sager et al. (US PAT. 6,425,055 hereinafter Sager).

Regarding claim 36, Cypher discloses a method of operating an associative cache having a plurality of memory locations (160A to 160N, figure 1), each of the plurality of memory locations having only a single word line associated therewith (figure 3). Cypher differs from the claimed invention in not specifically teaching to use multiple decoders to decode respective addresses provided to the cache. However, Sager teaches to perform way selection in parallel set field decoding in a multiple way cache memory using a multiple decoders to decode respective addresses provided to the cache in order to reduce the amount of time required to output a cache line (col. 2 line 63 through col. 4 line 18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Cypher in using multiple decoders to decode respective addresses provided to the cache, as per teaching of Sager, in order to reduce the amount of time required to output a cache line.

Regarding claims 37-38, Sager teaches to use multiple decoders to concurrently decode respective address provided to respective ones of the plurality of ways of the cache (col. 3 line 44 through col. 4 line 3).

Regarding claim 39, Cypher teaches to control at least one of the multiplxers to select one of the first and second addresses as its output while concurrently controlling another multiplexers to select the other of the first and second addresses as its output (col. 3 line 66 through col. 6 line 65).

Regarding claim 40, Sager teaches to use multiple decoders to decode respective addresses provided to respective ones of the plurality of ways of the cache (col. 4 lines 3-18).

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Smith, III et al. (US PAT. 6,339,813) discloses a memory system for permitting a processor access to a cache line while it is being filled and emptied to main memory, thereby facilitating simultaneously storage and access to two separate logical cache lines within one physical cache lines (abstract).

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Or faxed to:

(703) 308-6606

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Art Unit: 2186

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li



Art Unit 2186

  
MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 21